ABSTRACT

1.	This paper investigates the origins of sub-threshold slope degradation in vertical MOSFETs (v-MOSFETs) due to dry etching of the polysilicon surround gate.	
2.	Control v-MOSFETs exhibit a degradation of subthreshold slope as the channel length is reduced from 250 to 100 nm, with 100 nm transistors having a value of 125 mV/dec and a DIBL of 210 mV/V.	
3.	The effect of the polysilicon gate etch is investigated using a frame-gate architecture in which the polysilicon gate overlaps the side of the pillar, thereby protecting the channel from etch damage.	
4.	This device shows no degradation of short channel effects when the channel length is scaled and exhibits a near-ideal sub-threshold slope of 76 mV/dec and a DIBL of 33 mV/V at a channel length of 100 nm.	
5.	Gated diode measurements unambiguously demonstrate that this improved sub-threshold slope is due to the elimination of etch damage at the top and bottom of the pillar created during polysilicon gate etch.	
6.	An alternative method of eliminating dry etch damage is then investigated by optimizing the Fillet Local Oxidation (FILOX).	
7.	These devices give a sub-threshold slope of 81 mV/dec and a DIBL of 25 mV/V at a channel length of 100 nm.	
8.	The improved immunity to dry etch damage is due to the creation of a thick protective oxide at the top and bottom of the pillar during the FILOX process.	

ABSTRACT

1.	The Lorentzian-like noise induced by Electron Valence Band (EVB) tunneling has been investigated in nand p-channel multiple-gate field-effect transistors (MuGFETs), processed on silicon-on-insulator (SOI) and strained SOI (sSOI) substrates.	
2.	The effect has been studied for different back-gate and front-gate biases and as a function of the device geometry.	
3.	Similar as for wide fully depleted SOI transistors, this type of excess low-frequency noise is found when the back gate is biased in accumulation.	
4.	However, it is shown that the characteristic time constant of the Lorentzian cannot be modeled assuming a uniform EVB tunneling current across the gate area of the MuGFETs.	
5.	This indicates an impact of the three-dimensional nature of the device architecture on the so-called linear kink effects.	
6.	In addition, it is demonstrated that the tensile strain in sSOI MuGFETs also yields a change in the Lorentzian parameters, associated with changes in the EVB tunneling current.	

ABSTRACT

1.	This paper investigates, for the first time, the influence of high-energy neutrons on Multiple-Gate FETs (MuGFETs) with various gate lengths and fin widths	
2.	Neutron-induced degradation is addressed through the variation of major device parameters such as threshold voltage, subthreshold slope, maximum transconductance and DIBL.	
3.	We demonstrate that high-energy neutrons result in total-dose effects largely similar to those caused by c- and proton-irradiations.	
4.	It is shown that, contrarily to the generallybelieved immunity to irradiation, very short-channel MuGFETs can become extremely sensitive to the total-dose effect.	
5.	The possible reasons of such length-dependent neutron-induced degradation are discussed and finally related to gate edges.	